7th International Conference on Reliability and Safety Engineering (ICRSE2023)

# Reliability Optimization Assisted by NSGA-II Algorithm to Design a Full-bridge DC-DC Converter

**Seyed Mehdi Nouri [1], Mehdi Alemi Rostami [2*],Peyman Mohammadi [3]**

**1,2,3- Khayam Research Institute (KRI), Ministry of Science, Research, and Technology, Tehran, Iran.**

Corresponding author, Mehdi.alemi.rostami@gmail.com

***Abstract***

*Isolated DC-DC converters are commonly utilized in several systems, including distributed power generation systems, energy storage systems, and aircraft power conversion systems. This study involves designing a full-bridge DC-DC converter and enhancing its reliability using the NSGA-II algorithm. The study evaluates the impact of various parameters such as output power, switching frequency, transformer turn ratio, and input voltage on the converter's reliability performance. The reliability and mean time to failure are determined through a Markov reliability model that considers open and short circuit faults in all components. The converter component failure rates are calculated using the MIL-HDBK-217 standard. The results indicate an improvement in the converter's reliability performance.*

**Keyword:** DC-DC Switching Converter, Markov Model, NSGA-II, Objective Optimization, Reliability

## Introduction

Isolated DC-DC converters are frequently used in multiple fields related to power systems, such as distributed power generation, energy storage, and aircraft power conversion systems [1],[2]. These applications come with technical challenges, making it crucial to investigate isolated DC-DC converters. The most common types of isolated DC-DC converters include forward, push-pull, half-bridge, and full-bridge topologies, all of which feature rectifies on the secondary side of the transformer [3]. Of these configurations, a full-bridge DC-DC converter with phase-shifting capabilities is one of the most common DC-DC converters used in high-power applications [4].

On the other hand, semiconductors' unreliability in power converters, particularly DC-DC converters, is a widely acknowledged issue . Given this problem and the reliance of DC-DC converters on semiconductors, it is essential to design fault-tolerant structures that improve the system's reliability and availability [5]. Numerous research efforts have been documented in the literature that assesses and improve the performance of converters under various operating conditions and from various perspectives, such as reliability and mean time to failure (MTTF). The paper in [5] presents an interleaved full soft-switching DC-DC boost converter and compares its reliability performance to that of single-stage soft-switching and hard-switching boost converters. [6] evaluates a conventional buck-boost converter from a reliability and MTTF perspective. In [7], a reliability analysis of an isolated DC-DC converter in a backup power supply application is conducted, taking into account the impacts of current and voltage stresses, ambient and junction temperatures, and conduction and switching losses.

Assessing the performance of power electronic converters equipped with fault tolerance during their useful lifespan can be achieved by examining their MTTF [8] . The reliability and MTTF of a converter during the optimization process can be evaluated through various methods, such as fault tree analysis [9] and Monte Carlo simulation [10]. However, the Markov method has a distinct advantage over other methods. In [11] and [12], Markov models are employed to study the reliability performance of DC converters, including their power conditioning systems. In [13] the reliability of the proposed fault tolerant converter is evaluated using a Markov chain approach, in comparison to other conventional converters.

In addition to assessing the converter's performance, there is a significant potential to improve its reliability. Hence, the individual performance indexes must be balanced and improved using appropriate techniques. Numerous studies have been carried out to optimize the

converter's performance indexes using Genetic Algorithms (GA). In [14], a single objective genetic algorithm (GA) was used to optimize the efficiency of a bidirectional DC-DC converter, with the optimization variables being the duty cycle, output inductor, and current ripple ratio. In [15], the Non-dominated Sorting in Genetic Algorithms (NSGA-II) was applied to carry out multi-objective optimization of buck converters, which led to achieving high efficiency, reduced size, and low cost. [16] recommended utilizing NSGA-II to optimize the efficiency and compactness of dc-dc boost converters in embedded applications. Nonetheless, there is scarce literature that concentrates on designing a full-bridge DC-DC converter and utilizing NSGA-II to improve the converter's reliability.

The study describes the design of a full-bridge DC-DC converter and the optimization of its reliability using NSGA-II. The considered DC-DC converter is shown in Fig. 1. The NSGA-II optimization algorithm leverages an objective function to enhance reliability performance. The optimization algorithm considers the impact of various converter parameters, such as output power, switching frequency, transformer turn ratio, and input voltage during the optimization process. The Markov model is employed to assess the reliability and MTTF of the converter under short circuit (SC) and open circuit (OC) faults affecting all components. In this paper, the reliability of the converter is assessed using a Markov model that considers various conditions, including healthy,derated, and complete failure. The failure rate of the components is calculated using the MIL-HDBK-217's failure rate equations [17]. The parameters of the NSGA-II algorithm, such as population size, number of iterations, and crossover and mutation probabilities, are then configured to improve reliability. The results show that the reliability has increased.

The structure of the paper is as follows: Section 2 outlines the procedure for designing a full-bridge DC-DC converter. Section 3 deals with the basic evaluation of component failure rates and the Markov model of the desired converter. Section 4 focuses on defining the parameters of the NSGA-II algorithm that optimizes reliability. Section 5 analyzes the optimization results. Finally, Section 6 concludes the paper.

## Design of the Full-bridge DC-DC converter

Designing an electronic power converter involves specifying the required specifications, implementing the design process, considering design conditions, and utilizing predetermined design values. First, the required specifications of the desired full-bridge phase shifted Converter must be determined, and finally, these specifications must be estimated based on the performance of the designed Converter. The specifications of the studied Converter are presented in Table 1.

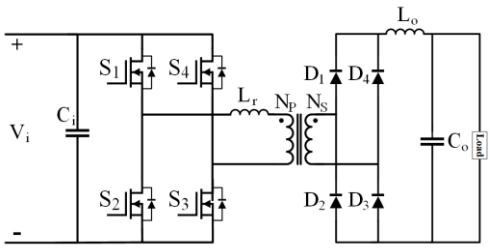



**Fig. 1** Structure of the Isolated Full-bridge DC-DC Converter

**Table 1.** Required Specifications for the Full-bridge DC-DC Converter

| Parameters | Unit | Value |
|---|---|---|
| Nominal output power($P_o$) | *kW* | 1.6 |
| Maximum output power($P_{o\text{-}max}$) | *kW* | 2 |
| Nominal output voltage ($V_o$) | *V* | 28 |
| Output voltage variation range | *V* | 26-30 |
| Nominal output current ($I_o$) | *A* | 57 |
| Output current variation range | *A* | 53-61 |
| Nominal input voltage ($V_i$) | *V* | 180 |
| Input voltage variation range | *V* | 150-200 |

The most important part of the design is to use design relationships step by step. During the implementation of the design process, some design conditions must be considered to control the design process to reach an acceptable result. During the design process, sometimes it is necessary to use predetermined coefficients and information, which are obtained based on design and manufacturing experiences. These coefficients, determined before the design and used during the design process, are referred to as design constraints. The design process of the desired power converter can be performed in the following order:

1. Obtaining initial design values.
2. Calculation of maximum and minimum transformer turns ratios.
3. Selection of an appropriate transformer turns ratio
4. Selection of appropriate Switching Frequency.
5. Modelling the transformer with averaging method: By using the averaging method during a complete cycle of key events, the performance of the transformer can be analyzed. The related relationships are described in detail in reference [18].
6. Calculating nominal voltage and current values of Components.
7. Calculating overall performance characteristics of the Converter under nominal condition [18] .
8. Calculating overall performance characteristics under overload conditions.

The analytical and simulation performance results of the designed converter are presented in Table 2.

**Table 2.** Specifications of a the Designed Full-bridge DC-DC converter

| Parameters | Unit | Analytical | Simulation |
|---|---|---|---|
| Nominal output voltage ($V_o$) | *V* | 28 | 27.9 |
| Output voltage ripple | *V* | 0.1 | 0.03 |
| Output voltage ripple in over-load | *V* | 0.15 | 0.1 |
| Switching frequency(f) | *kHz* | 60 | 60 |
| DC-link capacitor($C_i$) | *mF* | 3000 | 3000 |
| Transformer turns ratio ($n=N_p/N_s$) | | 4 | 4 |
| Output inductor($L_o$) | *mH* | 66 | 66 |
| Output capacitor($C_o$) | *μF* | 300 | 300 |
| Output power($P_o$) | *kW* | 1.6 | 1597 |
| Efficiency | *%* | 91 | 90 |
| Power factor | *%* | 98 | 98 |
| MTTF | *hour* | 29100 | 29000 |

## Evaluating Reliability

### Markov Model

In recent years, the Markov model has received much attention as a technique for evaluating converter reliability. The Markov model is a type of random process that is independent of past events and relies exclusively on the current state of the system [19]. A Markov model consists of possible states and their transition paths.

This section explains the reliability evaluation of the proposed DC-DC converter using Markov process models. The research provides the following steps for the reliability analysis:

1. Identifying the converter operating states under different fault conditions.
2. Developing Markov chain models for both short circuit (SC) and open circuit (OC) faults.
3. Calculating the failure rate of each component in each operating state.
4. Determining the reliability and MTTF metrics under both SC and OC fault conditions.
5. Evaluating the overall system reliability performance.

The operating states of the converter under SC and OC faults on its components are first identified. If there is an SC fault in the proposed converter design, it will result in a total system failure, represented as an absorbing state. In case of OC faults on some components, the converter can still function in other operating states with different power flow arrangements, represented as derated states.

Based on the identified operating states, the Markov chain structure for the proposed converter under SC and OC fault conditions is shown in Fig. 2 and the operating states are listed in Table 3.

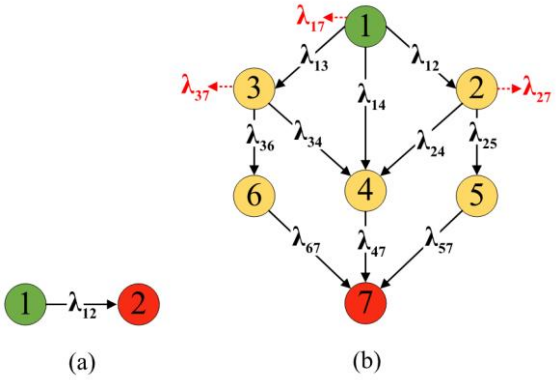



**Fig. 2.** Markov chain structure of the proposed converter under (a) short-circuit and (b) open-circuit fault scenarios.

**Table 3.** Specifications of different operating states under OC fault scenarios

| State | Condition | OC Fault on Components |
|---|---|---|
| 1 | *Healthy* | - |
| 2 | *Partial Power states* | $D_1$, $D_2$ , $D_3$, or $D_4$ |
| 3 | | $S_1$, $S_2$ , $S_3$, or $S_4$ |
| 4 | | $S_1$ or $S_3$ if $D_1$ or $D_3$ has failed<br>$S_2$ or $S_4$ if $D_2$ or $D_4$ has failed<br>$S_1$ or $S_3$ if $S_1$ or $S_3$ has failed<br>$S_2$ or $S_4$ if $S_2$ or $S_4$ has failed |
| 5 | | $D_1$&$D_3$ or $D_2$&$D_4$ |
| 6 | | $S_1$&$S_3$ or $S_2$&$S_4$ |
| 7 | *Absorbing* | - |

The transition from one operating state to another due to a faulted component is assigned a failure rate ($\lambda_{ij}$). It has been discovered that during SC fault conditions, state 2 becomes an absorbing state, and during OC fault conditions, state 7 becomes the absorbing state. According to Fig. 2(a), the only one failure rate ($\lambda_{12}$) under SC fault conditions is calculated as the sum of all failure rates of converter components and can be expressed as follows:

$$\lambda_{12}^{SC} = \lambda_{S1}^{SC} + \lambda_{S2}^{SC} + \lambda_{S3}^{SC} + \lambda_{S4}^{SC} + \lambda_{D1}^{SC} + \lambda_{D2}^{SC} + \lambda_{D3}^{SC} + \lambda_{D4}^{SC} + \lambda_{Trans}^{SC} + \lambda_{Lo}^{SC} + \lambda_{Ci}^{SC} + \lambda_{Co}^{SC} \quad (1)$$

Where the failure rates of the system's components, including switches, diodes, input and output capacitors, transformer, and output inductor are represented by the parameters under SC fault scenarios. The proposed converter exhibits different $\lambda_{ij}$ values for various operating states under OC faults, as depicted in Table 3 and Fig. 3(b). The state-space equation, with SC faults as the premise, is formulated in the following:

$$d/dt\left[P_1^{SC}(t)\ \ P_2^{SC}(t)\right]= \left[P_1^{SC}(t)\ \ P_2^{SC}(t)\right]\begin{bmatrix}-\lambda_{12}^{SC} & \lambda_{12}^{SC}\\ 0 & 0\end{bmatrix} \quad (2)$$

The probabilities of the converter being in operating states 1 and 2, under SC fault conditions, are represented by $P_1^{SC}(t)$ and $P_2^{SC}(t)$, respectively. Given that the converter is in a healthy state of operation at the start, the initial probabilities are set to be equal to:

$$[P_{sc}(0)]=\begin{bmatrix}1 & 0\end{bmatrix} \quad (3)$$

As state 2 is determined to be the absorbing state under SC faults, the reliability of the proposed converter in these scenarios can be determined by the probability of the first state as follows:

$$R_{SC}(t)=P_1^{SC}(t)=e^{-\lambda_{12}^{SC}t} \quad (4)$$

On the other hand, the equation for the state-space in cases where there are OC faults affecting the converter components is expressed as follows:

$$d/dt\left[P_1^{OC}(t)\ P_2^{OC}(t)\ldots P_7^{OC}(t)\right] =\left[P_1^{OC}(t)\ P_2^{OC}(t)\ldots P_7^{OC}(t)\right]\times[A] \quad (5)$$

Here, $P_1^{OC}(t)$ to $P_7^{OC}(t)$ represent the probabilities for operating states 1 to 7 under OC fault conditions, respectively, and [A] is equal to:

$$[A]=\begin{bmatrix}-k_1 & \lambda_{12} & \lambda_{13} & \lambda_{14} & 0 & 0 & \lambda_{17}\\ 0 & -k_2 & 0 & \lambda_{24} & \lambda_{25} & 0 & \lambda_{27}\\ 0 & 0 & -k_3 & \lambda_{34} & 0 & \lambda_{36} & \lambda_{37}\\ 0 & 0 & 0 & -k_4 & 0 & 0 & \lambda_{47}\\ 0 & 0 & 0 & 0 & -k_5 & 0 & \lambda_{57}\\ 0 & 0 & 0 & 0 & 0 & -k_6 & \lambda_{67}\\ 0 & 0 & 0 & 0 & 0 & 0 & 0\end{bmatrix} \quad (6)$$

Where $k_i$ represents the sum of all failure rates in row i, since the sum of all elements in each row of the matrix A must be zero. Similarly to equation (3), the initial probability for the state under OC fault scenarios is assumed as follows:

$$[P_{OC}(0)]=\begin{bmatrix}1 & 0 & \ldots & 0\end{bmatrix} \quad (7)$$

As shown in Fig. 2(b), the operating state 7 is the absorbing state when there are OC faults. Thus, the reliability of the proposed converter in these situations can be evaluated as follows:

$$R_{OC}(t)=\sum_{i=1}^{6}P_i^{OC}(t) \quad (8)$$

Additionally, the MTTF index, which represents the reliability of the proposed converter under SC and OC fault conditions, is computed as follows:

$$MTTF_{SC}=\int_0^\infty R_{SC}(t)dt \qquad MTTF_{OC}=\int_0^\infty R_{OC}(t)dt \quad (9)$$

Finally, the system reliability and the MTTF of the proposed converter topology are calculated as follows:

$$R(t)=\alpha R_{SC}(t)+(1-\alpha)R_{OC}(t) \quad (10)$$

$$MTTF=\int_0^\infty R(t)dt =\alpha.MTTF_{SC}+(1-\alpha).MTTF_{OC} \quad (11)$$

where *a* is the probability of SC fault occurrence. Statistics indicate that the probability of an SC fault occurring in power electronic semiconductor devices is greater than that of an OC fault [20]. Therefore, it is assumed that in the event of a switch or diode failure, there is a probability of 0.7 for it to be an SC fault and a probability of 0.3 for it to be an OC fault.

**Failure Rate**

The failure rate of the power converter components determines the likelihood of their malfunction. To perform a reliability analysis, it is crucial to compute the failure rate over the lifespan of the converter. Table 4 presents various factors that affect the failure rate of converter components, including the components' environmental conditions ($\pi_E$), design quality ($\pi_Q$), application factor ($\pi_A$), series resistance factor ($\pi_{SR}$), construction factor ($\pi_C$), and capacity factor ($\pi_{Cap}$). The formulated failure rate equations are derived from the military handbook MIL-HDBK-217F [17]. In this study, $\pi_Q$, $\pi_E$, $\pi_A$, and $\pi_C$ are considered equal to 5.5, 1, 8, and 1, respectively. Furthermore, the capacitor voltage stress factor ($\pi_V$) and the diode electrical stress factor ($\pi_S$) are as follows:

$$\pi_S=V_S^{2.43} \quad (12)$$

$$\pi_V=\left(\frac{S}{0.6}\right)^3 \quad (13)$$

where $V_S$ represents the ratio of the applied reverse voltage to the rated reverse voltage across the diode. Moreover, *S* denotes the ratio between the operating voltage and the rated voltage across the capacitor.

**Table 4.** Component Failure rates

| Component | Effective factors |
|---|---|
| Switch | $\lambda_{MOSFET} = \lambda_b \pi_T \pi_A \pi_Q \pi_E$ |
| Diode | $\lambda_D = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E$ |
| Transformer | $\lambda_T = \lambda_b \pi_T \pi_Q \pi_E$ |
| Inductor | $\lambda_I = \lambda_b \pi_T \pi_Q \pi_E$ |
| Capacitor | $\lambda_C = \lambda_b \pi_T \pi_V \pi_Q \pi_E \pi_{SR} \pi_{Cap}$ |

The component's temperature ($\pi_T$) is another critical factor responsible for the failure rates of the components, directly affected by the component's power loss ( $P_S^{Loss}$, $P_D^{Loss}$, $P_{Trans}^{Loss}$, and $P_{Ind}^{Loss}$ ). Table 5 shows the equivalent circuit diagram of the converter components and their relative power losses. Moreover, $\pi_T$ depends on the device junction temperature ($T_j$ ) for MOSFET and diode and the hot spot temperature (*THS)* for both inductor and transformer. The temperature factor $\pi_T$ for different parts of the converter, such as MOSFET, diode, inductor, and transformer are listed in table 5. According to junction and hot spot temperature equations, it can be concluded that higher power loss yields higher $T_j$ and $T_C$ temperatures which directly increases the value of the corresponding $\pi_T$. Additionally, it will reduce the reliability of converters by increasing the failure rate of components. The converter components in this study are all acquired from the available datasheets of IXFK30N50Q and MBR20050CT. Eventually, Table 6 presents numerical results demonstrating failure rates based on the explanation of the probable operation states of each SC or OC fault scenario.

The evaluation of the proposed converter's dependability in the presence of both SC and OC faults is carried out using equations (4) and (8), as outlined below:

$$R_{SC}(t) = = e^{-40.43t}$$
$$R_{OC}(t) = = 1.45e^{-60.61t} - 0.71e^{-39.88t} - 2.04e^{-20.67t} + 1.1e^{-10.16t} - e^{-0.31t} \quad (14)$$

**Table 6.** Calculated failure rates based on probable operation states of each SC or OC fault scenario

| Parameter | Value | Parameter | Value | Parameter | Value |
|---|---|---|---|---|---|
| $\lambda_{12}$ | 39.4 | $\lambda_{25}$ | 19.7 | $\lambda_{47}$ | 10.16 |
| $\lambda_{13}$ | 0.96 | $\lambda_{27}$ | 0.49 | $\lambda_{57}$ | 0.316 |
| $\lambda_{14}$ | 20.18 | $\lambda_{34}$ | 19.7 | $\lambda_{67}$ | 9.926 |
| $\lambda_{17}$ | 0.076 | $\lambda_{36}$ | 0.48 | $\lambda_{12}^{SC}$ | 40.43 |
| $\lambda_{24}$ | 0.48 | $\lambda_{37}$ | 19.7 | | |

## Optimization using NSGA-II

In this research, the NSGA-II algorithm is suggested as a technique for optimizing an objective function. This algorithm has been specially developed to handle complex objective formulations. One of the key difficulties of NSGA-II is determining the algorithm parameters such as the population size, number of iterations, crossover, and mutation probabilities, which are presented in Table 7. This study considers reliability as the objective function to optimize by minimizing the following function:

$$OF = \min\{MTTF_d - MTTF_c\} \quad (15)$$

where $MTTF_d$ is the desired MTTF value, selected to 40000 hours, and $MTTF_c$ is the computed MTTF through NSGA-II under each iteration of the optimization procedure. The algorithm optimizes the objective function by adjusting the value of converter parameters, such as inductance, capacitors, switching frequency, DC link voltages, and transformer turn ratio. This procedure continues to provide a satisfactory outcome.

**Table 7** NSGA-II parameter values

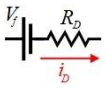
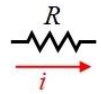
| Parameter | Value |
|---|---|
| Population size | 50 |
| Iterations | 50 |
| Crossover probability | 0.9 |
| Mutation probability | 0.3 |

## Results & Discussion

The simulation and optimization of the converter have been executed using the MATLAB software platform. Here we present an evaluation of the reliability performance of the full-bridge DC-DC power electronic converter, considering its operation in both

DCM and CCM modes.

**Table 5** Evaluation of the temperature factor on the converter components' failure rates

| Component | Circuit Model | Power Loss | Junction and Hot spot Temperature | Temperature Factor |
|---|---|---|---|---|
| Switch |  | $P_S^{Loss}=\frac{1}{T_S}\left[\int_0^{T_S} R_{DS,on} i_S^2(t)dt\right]+\left[C_0 f_S V_S^2\right]$ | $\begin{cases}T_J=T_C+\theta_{JC}P_S^{Loss}\\T_C=T_A+\theta_{CA}P_S^{Loss}\end{cases}$ | $\pi_T=\exp\left[-1925(\frac{1}{T_j+273}-\frac{1}{298})\right]$ |
| Diode |  | $P_D^{Loss}=\frac{1}{T_S}\left[\int_0^{T_S}(R_{D,on} i_D^2(t)+V_f i_D(t))dt\right]$ | $\begin{cases}T_J=T_C+\theta_{JC}P_D^{Loss}\\T_C=T_A+\theta_{CA}P_D^{Loss}\end{cases}$ | $\pi_T=\exp\left[-3091(\frac{1}{T_j+273}-\frac{1}{298})\right]$ |
| Inductor or Transformer |  | $P_{Trans}^{Loss}=P_{Ind}^{Loss}=\frac{1}{T_S}\left[\int_0^{T_S} Ri^2(t)dt\right]$ | $\begin{cases}T_{HS}=T_A+1.2\Delta T\\\Delta T=\frac{125P_{Trans}^{Loss}}{A}\end{cases}$ | $\pi_T=\exp\left[-1276(\frac{1}{T_{HS}+273}-\frac{1}{298})\right]$ |

It is important to mention that the optimization procedure does not include the leakage inductance of the transformer. Table 8 illustrates the optimal converter's parameters through NSGA-II. For the isolated full-bridge DC-DC converter, the optimized MTTF is equal to 40000 hours, and efficiency is 92%, reflecting improved reliability while maintaining high efficiency.

The assumed initial values for the output power, switching frequency, transformer turn ratio, time duration, input voltage, and output load are Po=1600W, fs=60 kHz, n=5, t=1.5×106Hr, Vi=185, and R=0.5, respectively. Assuming the switch and diode to be two sample semiconductors, their forward voltage drop and ON resistance are 1 V-0.1 Ω and 0.8 V-0.03 Ω, respectively. In the analysis provided, t is measured in hours multiplied by 106. The effect of the aforementioned parameters on the overall reliability performance is being investigated as follows:

**Table 7.** AC-DC converter optimized parameters and specifications

| Parameters | Unit | Values |
|---|---|---|
| PFC inductance($L_i$) | *mH* | 0.97 |
| Switching frequency($f_1$) | *kHz* | 60 |
| DC link capacitor($C_i$) | *μF* | 2200 |
| Nominal input voltage ($V_i$) | *V* | 185 |
| Transformer turns ratio ($n=N_p/N$) | - | 5 |
| Output inductor($L_o$) | *mH* | 55.5 |
| Output capacitor($C_o$) | *μF* | 200 |
| Efficiency | *%* | 92 |
| Power factor | *%* | 99 |
| MTTF | *hour* | 40000 |

- Output Pwer($P_o$):

  Designing power electronic converters requires considering the output power range as a significant parameter. This section explores how changes in output power (Po) affect the reliability performance of DC-DC converters, with Figs. 3(a) and (b) show the reliability performance of the DCM and CCM full-bridge converter, respectively. The evidence indicates that when the output power is increased, it results in greater circuit component losses, leading to a rise in the failure rate. Subsequently, this rise in the failure rate causes a reduction in reliability performance. To provide numerical results, the reliability performance of the CCM and DCM modes are demonstrated as reaching 0.44 and 0.56, respectively, at Po=1600W and t=0.04×106 hours. For further investigation, Fig. 7(a) displays the MTTF versus output power variations under different αS values. By increasing Po and αS, it is apparent that the MTTF reduces to lower values. The similar characteristics of reliability and MTTF metrics are because MTTF is obtained by integrating reliability over time (t).

- Input Voltage($V_i$):

  Power electronic devices have an inconsistent input voltage which can affect how well the converter operates. The reliability performance of the DC-DC converter is shown in Fig. 4, comparing its performance during DCM and CCM operations. The illustration indicates that the DCM has slightly lower reliability than the CCM, particularly under conditions of high Vi. This is attributed to the higher stress on components, increased power loss, raised operational temperature, and reduced reliability that occurs as Vi increases.

  The reason why the DCM has lower reliability than the CCM, particularly when the input voltage Vi is high, is because the DCM operates with a higher peak current in the switching devices, which results in increased switching losses and higher junction temperatures. As a consequence, the stress on the power devices and other components in the circuit is greater, leading to decreased reliability. In contrast, the CCM operates with a lower peak current and has less stress on the circuit components, making it more reliable. Additionally,

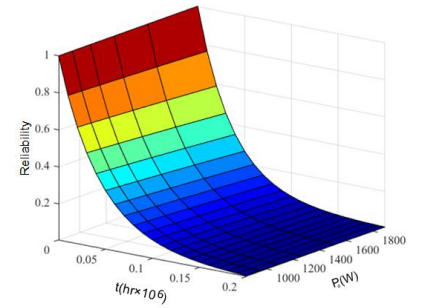
the DCM may experience a higher risk of electromagnetic interference (EMI) due to the higher peak current and fast-switching transitions, which could also contribute to decreased reliability. Fig. 7(b) displays the MTTF versus Vi under different αS values. According to the result, it is apparent that a greater level of reliability can be attained when Vi is greater than 170 and lower than 130.

- Transformer Turns Ratio(*n*):

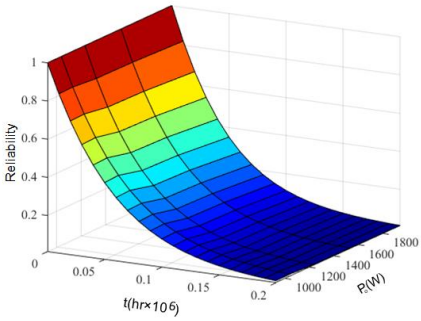
Choosing an optimal turn ratio for the transformer can greatly enhance the converter's overall reliability. If the value of n is too low, it results in higher output voltage levels and greater stress on the primary-side semiconductor current. Fig. 5 demonstrates the reliability performance of the converter as a function of n and t, with the CCM operation offering slightly higher reliability at a constant Po and varying n. According to the results, the reliability performance can be slightly enhanced by increasing the n. This is due to the fact that a higher turns ratio can lower the current passing through the switch and diodes, thereby reducing the thermal stress on these components and leading to greater reliability and an extended lifespan for the converter. Moreover, an increased turns ratio can also decrease the voltage stress on the switches and diodes, contributing to the further improvement of reliability performance. For further investigation, Fig. 7(c) displays the MTTF versus n under different αS values. The results demonstrate that increasing the n to a value greater than 6 can enhance reliability performance. However, in the present study, it is impossible to utilize such a high turns ratio due to the input and output voltage constraints.

- Switching Frequency ($f_{sw}$):

The switching frequency value can have an impact on the reliability performance of a full-bridge DC-DC converter. The reliability performance of the considered converter is shown in Fig. 6, comparing its performance during DCM and CCM operations. The findings indicate that the reliability of the converter decreases with an increase in switching frequency. Meanwhile, Fig. 7(d) shows the relationship between the MTTF and fsw at different αS values, and similarly indicates that αS the switching frequency increases, the MTTF of the converter decreases. Generally, a higher switching frequency can result in increased stress on the components, which may lead to reduced reliability. This is because higher switching frequencies can cause more switching losses and greater thermal stress on the components. On the other hand, a lower switching frequency can reduce stress on the components, potentially leading to improved reliability. Although a lower switching frequency may reduce stress on the converter's components, it can lead to higher output ripple and lower efficiency, which can cause increased stress on the components over time and potentially reduce their lifespan. Therefore, a balance must be struck between the benefits and drawbacks of low switching frequency to optimize reliability performance.

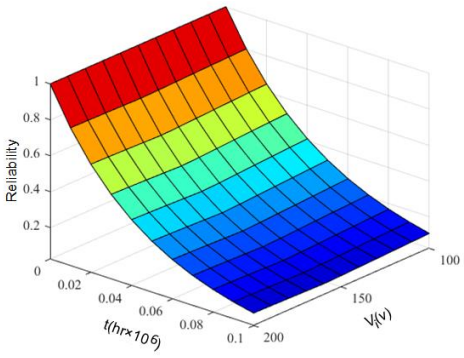



(a)

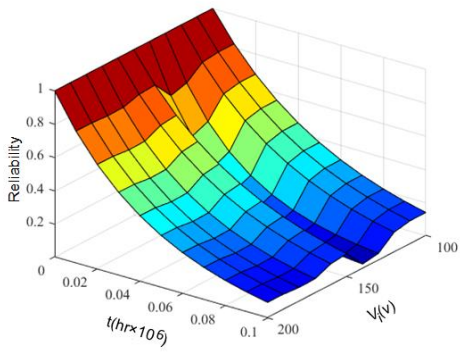



(b)

**Fig. 3.** Reliability of full-bridge converter with respect to $P_o$ and *t*. (a) DCM mode (b) CCM mode

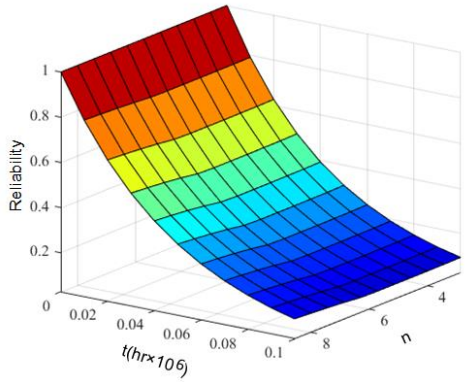



(a)

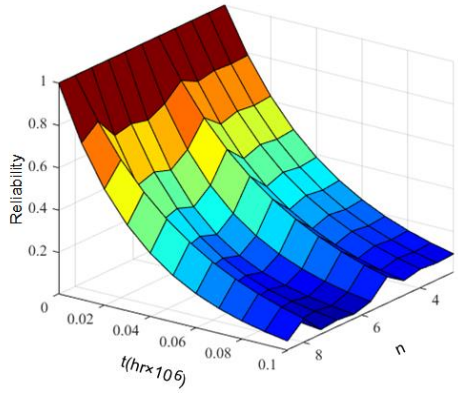



(b)

**Fig. 4.** Reliability of full-bridge converter with respect to $V_i$ and *t*. (a) DCM mode (b) CCM mode

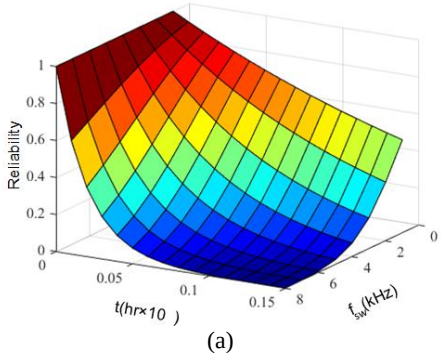



(a)

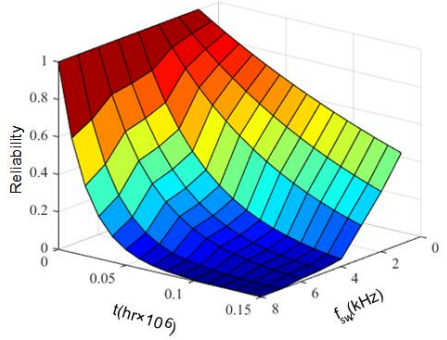



(b)

**Fig. 5.** Reliability of full-bridge converter with respect to *n* and *t*. (a) DCM mode (b) CCM mode

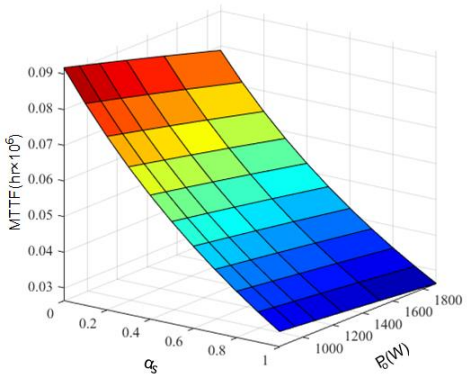



(a)

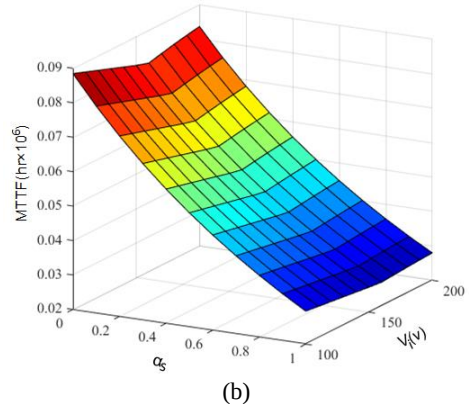



(b)

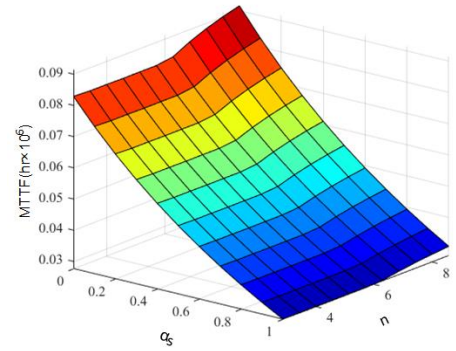
**Fig. 6.** Reliability of full-bridge converter with respect to $f_{sw}$ and *t*. (a) DCM mode (b) CCM mode



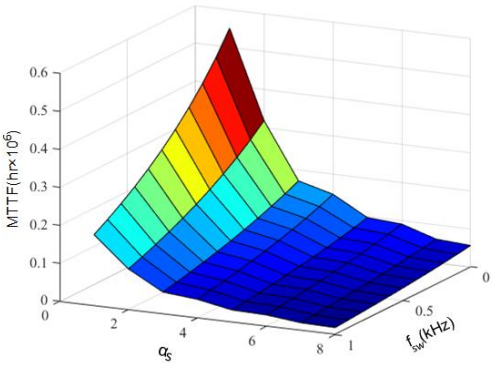

(a)




(b)




(c)




(d)

**Fig. 7.** Three-dimensional MTTF evaluation of the full-bridge converter under DCM mode with respect to $\alpha_S$ and: (a) $P_o$ (b) $V_i$ (c) $n$ (d) $f_{sw}$

## Conclusion

This paper has presented the design of a full-bridge DC-DC converter and the optimization of its reliability using markov model and NSGA-II algorithm. The objective of the NSGA-II optimization algorithm was to improve the converter's reliability by considering various parameters, such as output power, switching frequency, transformer turn ratio, and input voltage. The impact of these parameters was considered during the optimization process. The Markov model was employed to evaluate the converter's reliability and MTTF under both SC and OC fault scenarios. The analysis revealed that increases in the input voltage, switching frequency, and output power have an adverse impact on the converter's MTTF and overall reliability performance. Based on the optimization results, the converter's MTTF and efficiency of 40,000 hours and 92% were obtained, indicating an increase in reliability performance and efficiency.

## References

[1] Y. Azadeh, E. Babaei, H. Tarzamni, and M. Sabahi, "Single-inductor dual-output DC–DC converter with capability of feeding a constant power load in open-loop manner," IEEE Transactions on Industrial Electronics, vol. 66, no. 9, pp. 6906-6915, 2018.

[2] M. Hossain and N. Rahim, "Recent progress and development on power DC-DC converter topology, control, design and applications: A review," Renewable and Sustainable Energy Reviews, vol. 81, pp. 205-230, 2018.

[3] R. Jeyapradha and V. Rajini, "Comparison of Isolated DC-DC Converters for Low/Medium Voltage Solid State Transformer applications," Journal of Electrical and Electronics Engineering, vol. 15, no. 1, pp. 39-45, 2022.

[4] H. He, Y. Liu, C. Wang, and C. Zhang, "Design of Digital Control Phase-Shifting Full-Bridge Switching Power Supply," in IOP Conference Series: Materials Science and Engineering, 2019, vol. 533, no. 1, p. 012036: IOP Publishing.

[5] H. Tarzamni, E. Babaei, A. Zarrin Gharehkoushan, and M. Sabahi, "Interleaved full ZVZCS DC–DC boost converter: analysis, design, reliability evaluations and experimental results," IET Power Electronics, vol. 10, no. 7, pp. 835-845, 2017.

[6] H. Tarzamni, F. Tahami, M. Fotuhi-Firuzabad, and F. P. Esmaeelnia, "Reliability analysis of buck-boost converter considering the effects of operational factors," in 2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2019, pp. 647-652: IEEE.

[7] S. Peyghami, H. Wang, P. Davari, and F. Blaabjerg, "Mission-profile-based system-level reliability analysis in DC microgrids," IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 5055-5067, 2019.

[8] R. Faraji, L. Ding, T. Rahimi, and M. Kheshti, "Application of soft-switching cell with inherent redundancy properties for enhancing the reliability of boost-based DC–DC converters," IEEE Transactions on Power Electronics, vol. 36, no. 11, pp. 12342-12354, 2021.

[9] Y.-Y. Hong, L.-H. Lee, and H.-H. Cheng, "Reliability assessment of protection system for switchyard using fault-tree analysis," in 2006 International Conference on Power System Technology, 2006, pp. 1-8: IEEE.

[10] Y. Zhao, Y. Tang, W. Li, and J. Yu, "Composite power system reliability evaluation based on enhanced sequential cross-entropy Monte Carlo simulation," IEEE Transactions on Power Systems, vol. 34, no. 5, pp. 3891-3901, 2019.

[11] H. Tarzamni, F. Tahami, M. Fotuhi-Firuzabad, and F. Blaabjerg, "Improved Markov model for reliability assessment of isolated multiple-switch PWM DC-DC converters," IEEE Access, vol. 9, pp. 33666-33674, 2021.

[12] S. Raj, V. Singh, N. K. Rajalwal, and D. Ghosh, "Reliability prediction of a distribution protection scheme using Markov model," in 2020 8th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions)(ICRITO), 2020, pp. 868-872: IEEE.

[13] T. Rahimi, S. H. Hosseini, M. Sabahi, G. B. Gharehpetian, and M. Abapour, "Reliability evaluation of a fault-tolerant three-phase interleaved DC-DC boost converter," Transactions of the Institute of Measurement and Control, vol. 41, no. 5, pp. 1278-1289, 2019.

[14] C.-K. Chew and S. R. R. Kondapalli, "Modeling, Analysis, Simulation and Design Optimization (Genetic Algorithm) of dc-dc Converter for Uninterruptible Power Supply Applications," in 2005 International Conference on Power Electronics and Drives Systems, 2005, vol. 2, pp. 1530-1535: IEEE.

[15] W. Chang, J. Wang, and Q. Chen, "Multi-objective optimization of synchronous buck converter based on NSGA-U algorithm," in 2016 IEEE International Conference on Mechatronics and Automation, 2016, pp. 1391-1395: IEEE.

[16] D. Dell'Isola, M. Urbain, M. Weber, S. Pierfederici, and F. Meibody-Tabar, "Optimal design of a DC–DC boost converter in load transient conditions, including control strategy and stability constraint," IEEE Transactions on Transportation Electrification, vol. 5, no. 4, pp. 1214-1224, 2019.

[17] U. DoD, "MIL-HDBK-217F (N2), Reliability Prediction of Electronic Equipments," US Department of Defense, 1995.
[18] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of DC–DC converter systems," IEEE Transactions on Power Electronics, vol. 24, no. 1, pp. 288-300, 2009.
[19] M. A. Boyd and S. Lau, "An introduction to Markov modeling: Concepts and uses," in Annual Reliability and Maintainability Symposium, 1998.
[20] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters-an overview," in IECON 2013-39th Annual Conference of the IEEE Industrial Electronics Society, 2013, pp. 507-513: IEEE.